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Information processing systems — Information exchange between systems — Synchronous transmission signal quality at DTE/DCE interfaces

Systèmes de traitement de l'information — Échange d'informations entre systèmes — Qualité des signaux en transmission synchrone à l'interface ETTD/ETCD

Reference number
ISO 9543 : 1989 (E)

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

Draft International Standards adopted by the technical committees are circulated to the member bodies for approval before their acceptance as International Standards by the ISO Council. They are approved in accordance with ISO procedures requiring at least 75 % approval by the member bodies voting.

International Standard ISO 9543 was prepared by Technical Committee ISO/TC 97, *Information processing systems.*

Annex A of this International Standard is for information only.

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Information processing systems — Information exchange between systems — Synchronous transmission signal quality at DTE/DCE interfaces

1 Scope

1.1 This International Standard specifies signal quality requirements for serial data transmission at the interface between synchronous transmission Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE). The interface referred to in this International Standard conforms to CCITT Recommendations V.24 (telephone networks), X.24 (data networks) as specified in DCEs of CCITT Recommendations:

V.22, V.22bis, V.23, V.26. V.26bis, V.26ter, V.27, V.27bis, V.27ter, V.29, V.32, V.33, or

X.21bis together with V.28, electrical characteristics; or

V.35 together with V.28/V.35 electrical characteristics; or

V.36, V.37 or X.21 together with V.10/V.11, electrical characteristics; or

X.22 together with V.11, electrical characteristics.

It is also recognized and considered that during the evolution of ISDN there will exist V.-series and X.-series type interfaces at ISDN Reference point R, as specified in CCITT Recommendations V.110, X.30 and X.31.

The speed limitation is determined by the referenced CCITT DCE Recommendations in the X. (e.g. X.10) and V. (e.g. V.5, V.6) series.

The signal quality requirement is limited to synchronous transmission at the interface with synchronous DCEs. Signal quality pertaining to asynchronous DTEs is not part of this International Standard.

1.2 This International Standard recognizes the need to have performance categories of signal quality depending on the type of interchange circuits used at the interface for signal element timing. Two classes of timing, codirectional timing and contradirectional timing, are considered.

The signal quality is categorized by measurements of timing displacement between data and timing signals, of jitter, duty cycle, and accuracy of the timing signals. Application to ISDN Reference point S/T is excluded.

1.3 This International Standard is of particular importance when the interconnected equipment is furnished by different organizations. It does not attempt to indicate what action, if any, is to be taken if the limits are not met, but it is intended to provide a basis for agreement between parties involved.

1.4 This International Standard does not describe the signal quality of the DCE or the line associated with it. Neither does it describe any requirement for an acceptable bit error rate.

1.5 This International Standard may also be used for DTE to DTE direct connections when the referenced CCITT Interfaces are applied.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO 1282-9 : 1984, *Data processing — Vocabulary — Part 09: Data communication.*

CCITT Recommendation V.5 : 1984, *Standardization of data signalling rates for synchronous data transmission in the general switched telephone network.*

CCITT Recommendation V.6 : 1984, *Standardization of data signalling rates for synchronous data transmission on leased telephone-type circuits.*

CCITT Recommendation V.10 (= X.26) : 1984, *Electrical characteristics for unbalanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications.*

CCITT Recommendation V.11 (= X.27) : 1984, *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications.*

CCITT Recommendation V.22 : 1984, *1 200 bits per second duplex modem standardized for use on the general switched telephone network and on point-to-point 2-wire leased circuits.*

CCITT Recommendation V.22*bis* : 1984, *2 400 bits per second duplex modem using the frequency division technique standardized for use on the general switched telephone network and on point-to-point 2-wire leased telephone-type circuits.*

CCITT Recommendation V.23 : 1984, *600/1 200 baud modem standardized for use in the general switched telephone network.*

CCITT Recommendation V.24 : 1984, *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment.*

CCITT Recommendation V.26 : 1984, *2 400 bits per second modem standardized for use on 4-wire leased telephone-type circuits.*

CCITT Recommendation V.26*bis* : 1984, *2 400/1 200 bits per second modem standardized for use in the general switched telephone network.*

CCITT Recommendation V.26*ter* : 1984, *2 400 bits per second duplex modem using the echo cancellation technique standardized for use on the general switched telephone network and on point-to-point 2-wire leased telephone-type circuits.*

CCITT Recommendation V.27 : 1984, *4 800 bits per second modem with manual equalizer standardized for use on leased telephone-type circuits.*

CCITT Recommendation V.27*bis* : 1984, *4 800/2 400 bits per second modem with automatic equalizer standardized for use on leased telephone-type circuits.*

CCITT Recommendation V.27*ter* : 1984, *4 800/2 400 bits per second moderm standardized for use in the general switched telephone network.*

CCITT Recommendation V.28 : 1984, *Electrical characteristics for unbalanced double-current interchange circuits.*

CCITT Recommendation V.29 : 1984, *9 600 bits per second modem standardized for use on point-to-point 4-wire leased telephone-type circuits.*

CCITT Recommendation V.32 : 1984, *A family of 2-wire, duplex modems operating at data signalling rates of up to 9 600 bit/s for use on the general switched telephone network and on leased telephone-type circuits.*

CCITT Recommendation V.33 : 1984, *14 400 bits per second modem standardized for use on point-to-point 4-wire leased telephone-type circuits.*

CCITT Recommendation V.35 : 1984, *Data transmission at 48 kilobits per second using 60-108 kHz group band circuits.*

CCITT Recommendation V.36 : 1984, *Modems for synchronous data transmission using 60-108 kHz group band circuits.*

CCITT Recommendation V.37 : 1984, *Synchronous data transmission at a data signalling rate higher than 72 kbit/s using 60-108 kHz group band circuits.*

CCITT Recommendation V.110 : 1984, *Support of data terminal equipments (DTEs) with V-series type interfaces by an integrated services digital network (ISDN).*

CCITT Recommendation X.10 : 1984, *Categories of access for data terminal equipment (DTE) to public data transmission services provided by PDNs and/or ISDNs through terminal adaptors.*

CCITT Recommendation X.21 : 1984, *Interface between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) for synchronous operation on public data networks.*

CCITT Recommendation X.21*bis* : 1984, *Use on public data networks of data terminal equipment (DTE) which is designed for interfacing to synchronous V-series modems.*

CCITT Recommendation X.22 : 1984, *Multiplex DTE/DCE interface for user clases 3-6.*

CCITT Recommendation X.24 : 1984, *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks.*

CCITT Recommendation X.30 : 1984, *Support of X.21 and X.21bis based data terminal equipments (DTEs) by an integrated services digital network (ISDN).*

CCITT Recommendation X.31 : 1984, *Support of packet mode terminal equipment by an ISDN.*

3 Definitions

For the purposes of this International Standard, the definitions given in ISO 2389-9 and the following definitions apply.

3.1 codirectional timing: A configuration in which a timing signal and associated binary signals (data or control) are transferred in the same direction across the interface (see figure 7).

3.2 contradirectional timing: A configuration in which a timing signal and associated binary signals (data or control) are transferred in opposite directions across the interface (see figure 8).

3.3 signal element timing: A signal used to determine the duration of signal elements and to achieve synchronization within a synchronous transmission system.

3.4 timing displacement: Time to the unit interval between significant transitions of signal element timing and associated bit transitions of data. The degree of displacement is usually expressed as a percentage.

3.5 duty cycle: In signal element timing the duration of the signal condition from which a significant transition is originated. The duration is usually expressed as a percentage of the unit interval.

3.6 signal element: Each of the parts constituting a telegraph or data signal and distinguished from the others by its nature, magnitude, duration and relative position (or by one or some of these features only).

3.7 significant instants: The instants at which the successive significant conditions recognized by the appropriate device of the modulation or restitution begin.

Each of the instants is determined as soon as the appropriate device takes up the significant condition usable for a recording or a processing.

3.8 significant interval: Time interval between two consecutive significant instants.

3.9 jitter: The degree of short term variation of the significant instant of a digital signal from its ideal position in time.

3.10 transition: A change from one significant condition to another in a telegraph or a data signal.

3.11 data signalling rate: The aggregate of the number of binary digits (bits) per second in the transmission path of a data transmission system. (See the notes to definition 09.06.01 of ISO 2382-9 : 1984.)

3.12 serial transmission: The sequential transmission of the signal elements of a group representing a character or other entity of data. (See definition 09.03.04 of ISO 2382-9 : 1984.)

3.13 synchronous transmission: Data transmission in which the time of occurrence of each signal representing a bit is related to a fixed time base. (See definition 09.03.12 of ISO 2382-9 : 1984.)

3.14 synchronous DCE: The DCE is considered to be synchronous if signal element timing is exchanged at the interface of both the transmitting and receiving DTE.

4 Data signalling rate characteristics

The nominal value of the data signalling rate is application dependent and therefore not part of this International Standard.

5 Signal quality from the transmitting DTE

The interchange circuits associated with the transmit direction of synchronous DTEs should operate within the specified quality category as shown in table 1. The alphabetical designations in the following subclauses refer to the values specified in table 1.

For simplicity of presentation, signal quality requirements are specified separately in the transmit direction and the receive direction. It should be noted that circuit S is applicable in both cases, the relevant assigned quality values being identical.

Figure 9 illustrates the signal quality parameters on interchange circuits associated with the transmit direction.

5.1 Jitter on circuit 114 or S

The significant transitions of signal element timing on interchange circuit 114 of V.24 or S of X.24 are specified in figure 9[1]. They shall not have a jitter greater than B % of the unit interval at the actual data signalling rate, for an observation period of 10 s. The measurement is to be taken after the test arrangement has stabilized.

NOTE — Significant transitions for circuit S are specified differently for contradirectional and codirectional cases.

5.2 Jitter on circuit 113 or X

The significant transitions of signal element timing on interchange circuit X of X.24 or 113 of V.24 are specified in figure 9. They shall not have a jitter greater than B % of the unit interval at the actual data signalling rate, for an observation period of 10 s. The measurement is to be taken after the test arrangement has stabilized.

5.3 Duty cycle of signal element timing

The duty cycle of signal element timing on interchange circuits X, S, 113, 114 shall be C % of the unit interval.

5.4 Signal element timing accuracy

The data signalling rate on interchange circuits X, S, 113, 114 shall not deviate by more than D % from the nominal data signalling rate.

5.5 Timing displacement between circuits having codirectional timing relationships

The degree of displacement between associated transitions on the interchange circuits shall not be less than E % (see annex A).

5.6 Timing displacement between circuits having contradirectional timing relationships

The degree of displacement between associated transitions on the interchange circuits shall not be greater than F % (see annex A).

6 Signal quality at the receiving DTE

The interchange circuits associated with the receive direction of synchronous DTEs shall operate within the specified sytem quality category as shown in table 1. The alphabetical designations in the following subclauses refer to the value specified in table 1.

Figure 10 illustrates the various signal quality parameters on interchange circuits associated with the receive direction.

6.1 Jitter on circuit 128

The significant transitions of signal element timing on interchange circuit 128 of V.24 are specified in figure 10. They shall not have a jitter greater than G % of the unit interval at the actual data signalling rate, for an observation period of 10 s. The measurement is to be taken after the test arrangement has stabilized.

6.2 Jitter on circuit 115 or S

The specified significant transitions of signal element timing on interchange circuit 115 of V.24 or S of X.24 are specified in figure 10[1]. They shall not have a jitter greater than H % of the unit interval at the actual data signalling rate, for an observation period of 10 s. The measurement is to be taken after the test arrangement has stabilized.

NOTE — Significant transitions for circuit S are specified differently for contradirectional and codirectional cases.

6.3 Duty cycle of signal element timing

The duty cycle of signal element timing in interchange circuits S, 115, 128 shall be I % of the unit interval.

6.4 Signal element timing accuracy

The data signalling rate on interchange circuits S, 115, 128 shall not deviate more than J % from the nominal data signalling rate.

6.5 Timing displacement between circuits having contradirectional timing relationsips

The degree of displacement between associated transitions on the interchange circuits shall not be greater than K % (see annex A).

6.6 Timing displacement between circuits of codirectional timing relationships

The degree of displacement between associated transitions on the interchange circuits shall not be less than L % (see annex A).

7 Measurements at the interchange point

Measurements of the signal quality should meet one out of three sets of requirements depending on whether the electrical interface characteristics comply with the CCITT Recommendation V.28 or V.10 (= X.26) or V.11 (= X.27).

For measurements of data and timing circuits of V.35, provisionally the V.11 electrical characteristics may be considered equivalent for this purpose.

7.1 Measurement of the V.28 generator characteristics

7.1.1 Use of standard test load

The signal quality should be measured on the particular interchange circut concerned at the generator side while the circuit is terminated with the standard test load. This standard test load may be the input impedance of the device or may be an external device, but in all cases the total load on the interchange circuit should meet the requirements of 7.1.2.

7.1.2 Specification of the standard test load

The standard test load should consist of 3 000 Ω resistance shunted by 2 500 pF capacitance and should be connected from the signal interchange circuit under test to CCITT circuit 102 or circuit Ga or circuit Gb as shown in the test arrangement of figure 1.

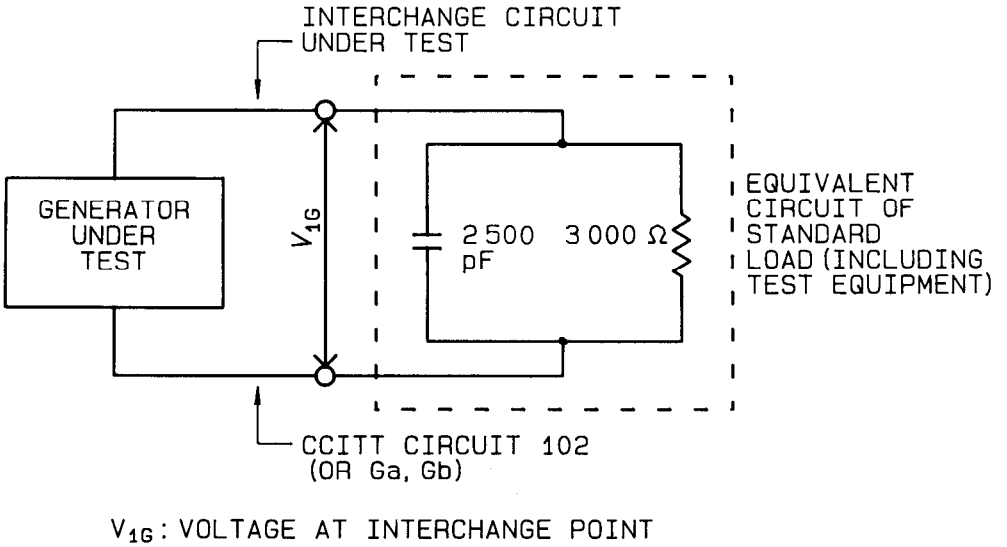


Figure 1 — Test arrangement for V.28 generators

7.1.3 Signal quality from the transmitting DTE

The signal quality measurements should be made using a + 3,0 V and a − 3,0 V threshold to determine the occurrence of signal transitions.

A binary 1 — to — binary 0 (OFF-to-ON) transition should be taken to occur at the instant V_{1G} crosses + 3 V on a positive going transition.

A binary 0 — to — binary 1 (ON-to-OFF) transition should be taken to occur at the instant V_{1G} crosses − 3 V on a negative going transition.

7.2 Measurements on the V.28 load side

7.2.1 Test arrangement

Measurements of signal quality on the load side of the interface should be made using the test arrangement of figure 2.

7.2.2 Signal quality at receiving DTE

The signal quality should be measured using a signal V_{1L} of ± 5,0 V when working into the load under test. The deviations of the transition in time should be taken to occur when the signal crosses the ± 3,0 V thresholds.

7.3 Measurement of the V.10 generator characteristics

7.3.1 Use of standard test load

The signal quality should be measured on the particular interchange circuit concerned at the generator side while the circuit is terminated with a standard test load. This standard test load may be the input impedance of the device or may be an external device but in all cases the total load on the interchange circuit should meet the requirements of 7.3.2.

7.3.2 Specification of the standard test load

The standard test load consists of 450 Ω resistance shunted by a capacitance C_w and should be connected from the signal interchange circuit under test to signal common return as shown in the test arrangement of figure 3. The value of C_w depends on the data signalling rate and should be the value given in the table annexed to figure 3 but reduced by the value of any capacitance included in the generator wave shaping.

7.3.3 Signal quality from the transmitting DTE

The measurements should be made using thresholds in the range ± 0,3 V to determine the occurrence of signal transitions. A threshold at nominal 0 V is preferred.

7.4 Measurement on the V.10 load side

7.4.1 Test arrangement

Measurements of signal quality on the load side of the interface should be made using the test arrangement of figure 4.

7.4.2 Signal quality at receiving DTE

The measurements should be made using a signal V_{1L} of ± 4,0 V when working into the load under test.

The deviations of the transitions in time should be taken to occur when the signal crosses the thresholds (see 7.3.3).

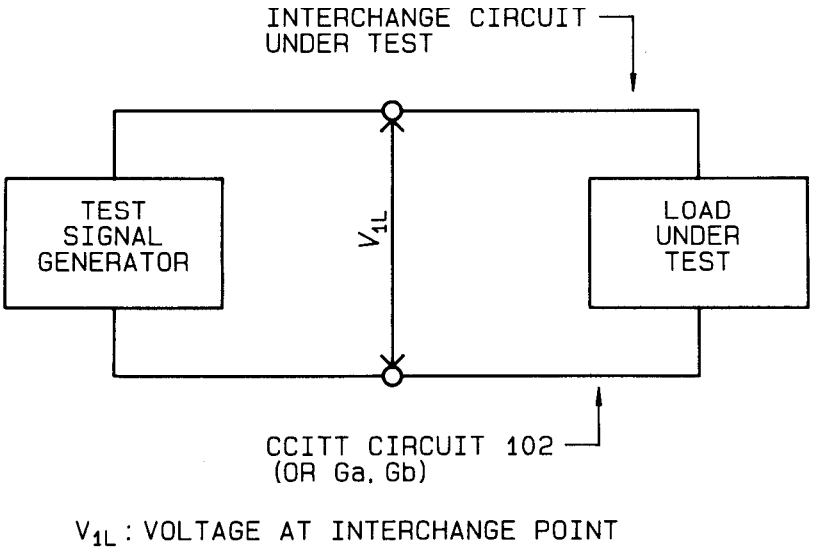
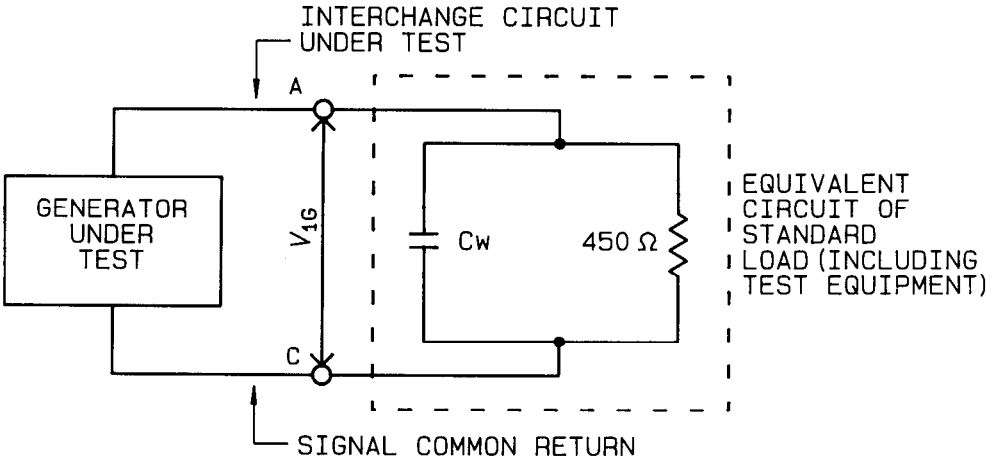


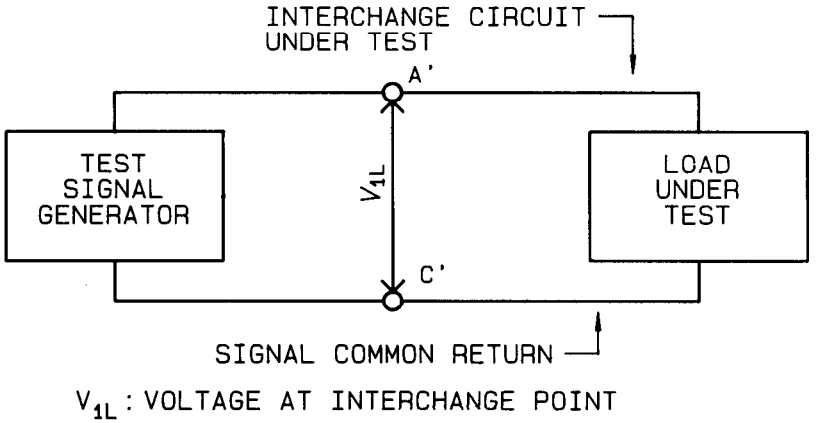
Figure 2 — Test arrangement for V.28 loads



V_{1G} : VOLTAGE AT INTERCHANGE POINT

Cw (uF)	DATA SIGNALLING RATE (k bit/s)		
1, 000	0	TO	2, 5
0, 470	2, 5	TO	5, 0
0, 220	5, 0	TO	10, 0
0, 100	10, 0	TO	25, 0
0, 047	25, 0	TO	50, 0
0, 022	50, 0	TO	100, 0

Figure 3 — Test arrangement for V.10 generators and values of Cw



V_{1L} : VOLTAGE AT INTERCHANGE POINT

Figure 4 — Test arrangement for V.10 loads

7.5 Measurement of the V.11 generator characteristics

7.5.1 Use of standard test load

The signal quality should be measured on the particular interchange circuit concerned at the generator side while the circuit is terminated with a standard test load. This standard test load may be the input impedance of the test device or may be an external device but in all cases the total load on the interchange circuit should meet the requirements of 7.5.2.

7.5.2 Specification of the standard test load

The standard test load should consist of 100 Ω resistance and should be connected between the output points A and B of the generator under test as shown in the test arrangement of figure 5.

7.5.3 Signal quality from the transmitting DTE

The measurements should be made using thresholds in the range ± 0,3 V to determine the occurrence of signal transitions. A threshold at nominal 0 V is preferred.

7.6 Meaurement on the V.11 load side

7.6.1 Test arrangement

Measurements of signal quality on the load side of the interface should be made using the test arrangement of figure 6.

7.6.2 Signal quality at receiving DTE

The measurements should be made using a signal V_{1L} of ± 4,0 V when working into the load under test.

The deviations of the transitions in time should be taken to occur when the signal crosses the thresholds (see 7.5.3).

7.7 Accuracy of measuring equipment

This International Standard does not specify the tolerances of the standard test loads or the accuracy of the measuring equipment or test signal generator.

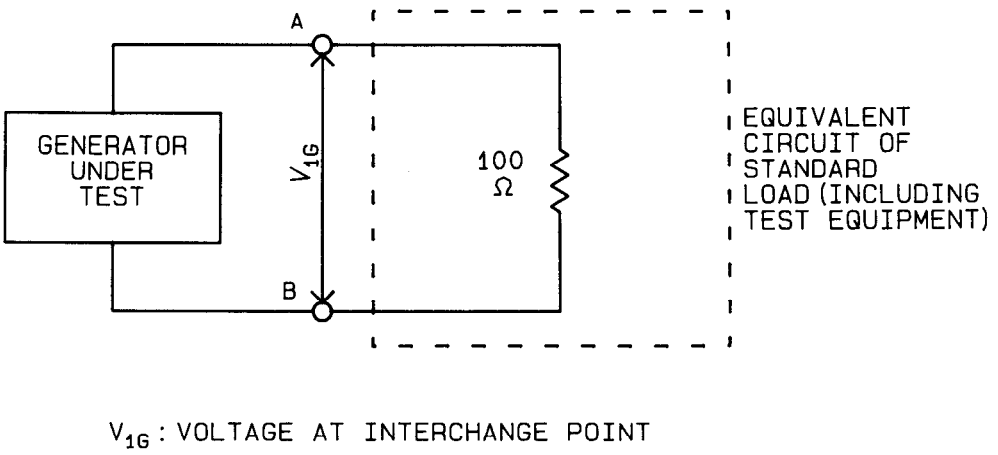


Figure 5 — Test arrangement for V.11 generators

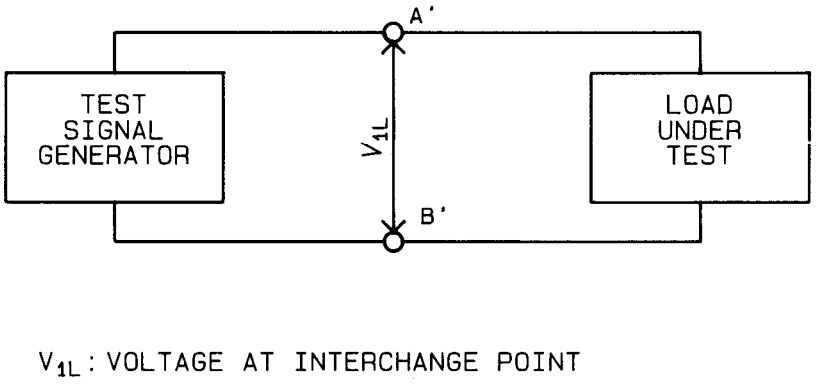


Figure 6 — Test arrangement for V.11 loads

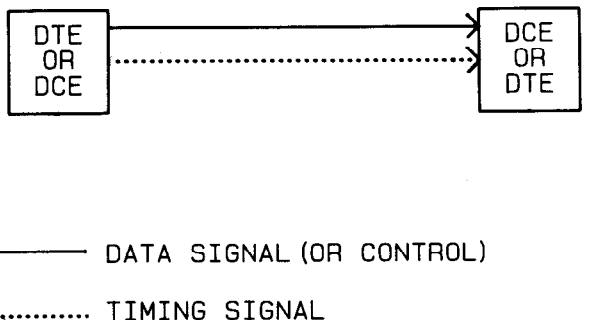


Figure 7 — Codirectional timing

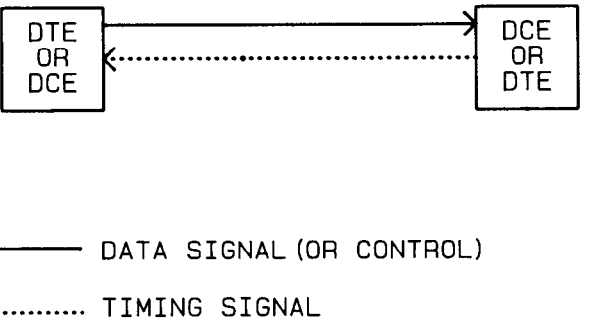


Figure 8 — Contradirectional timing

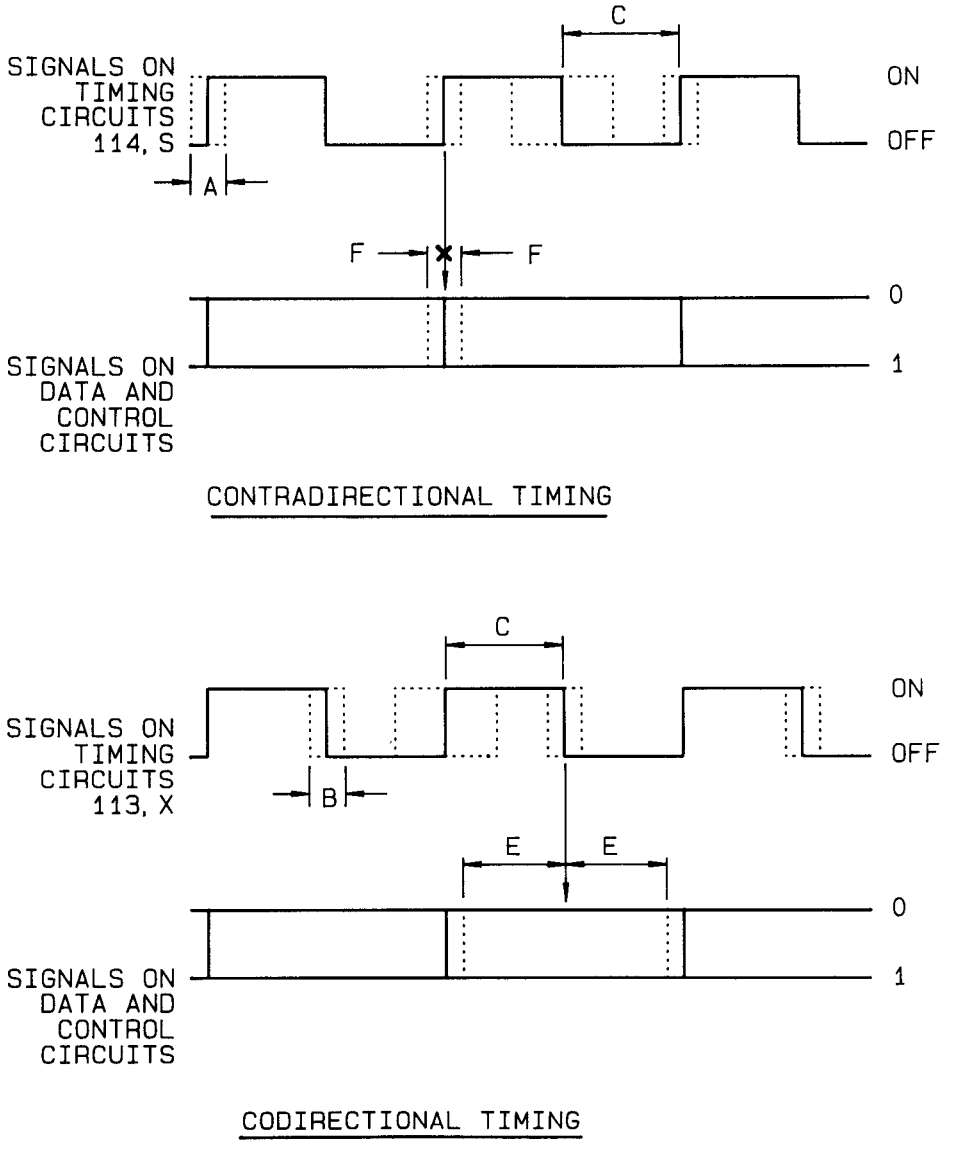
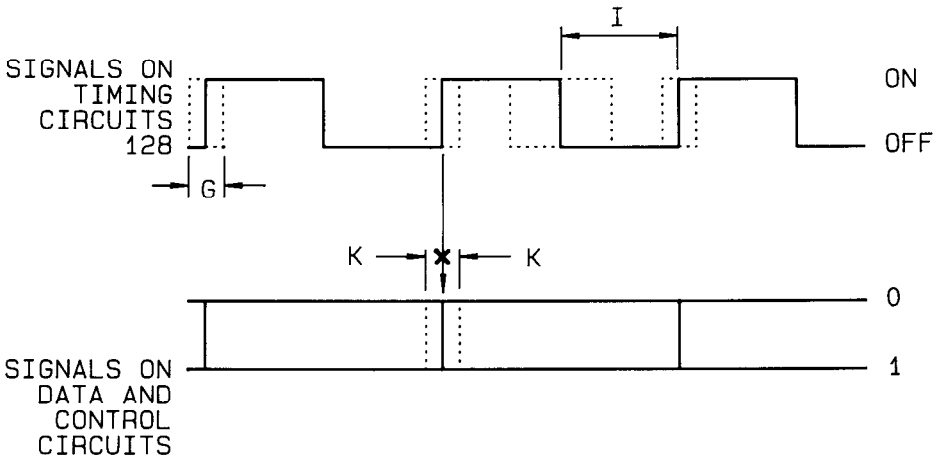


Figure 9 — Illustration of signal quality parameters on interchange circuits associated with the transmit direction



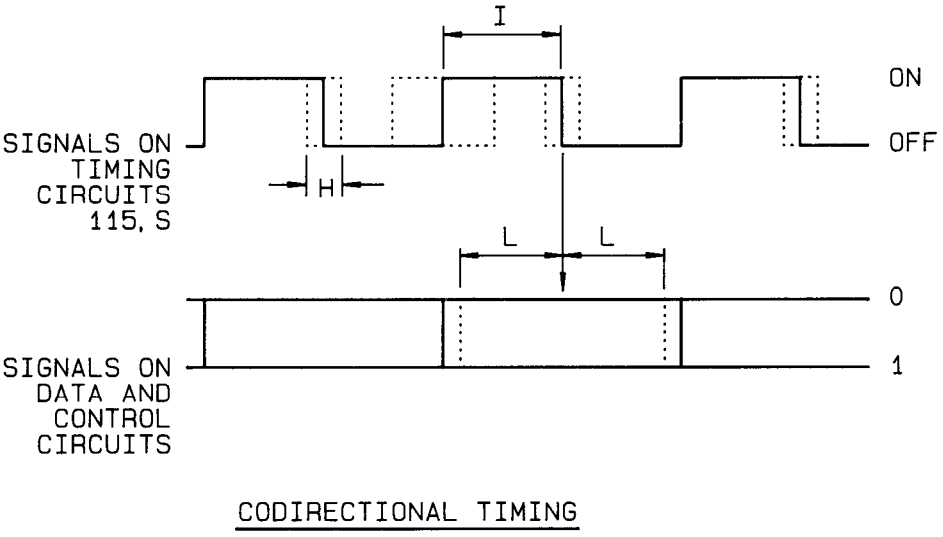


Figure 10 — Illustration of signal quality parameters on interchange circuits associated with the receive direction

Table 1 — Signal quality characteristics [1)]

DTE	Subclause	Designation	Symbol	Unit	Timing	
					Contradirectional	Codirectional
Transmitting DTE	5.1	Jitter	A	%	30 [2)]	—
	5.2	Jitter	B	%	—	1
	5.3	Signal element timing duty cycle	C	%	50 ± 10	50 ± 10
	5.4	Signal element timing accuracy	D	%	± 0,01 [3), 4)]	± 0,01 [3), 4)]
	5.5	Timing displacement (codirectional)	E	%	—	45
	5.6	Timing displacement (contradirectional)	F	%	10	—
Receiving DTE	6.1	Jitter	G	%	10	—
	6.2	Jitter	H	%	—	30 [2)]
	6.3	Signal element timing duty cycle	I	%	50 ± 10	50 ± 10
	6.4	Signal element accuracy	J	%	± 0,01 [4)]	± 0,01 [4)]
	6.5	Timing displacement (contradirectional	K	%	10	—
	6.6	Timing displacement (codirectional)	L	%	—	20

1) When categorizing signal quality of DTEs using the table, data signalling rate, operating mode, and environment conditions may be indicated for completeness.

2) The value of 30 % takes into account the fact that the signal element timing may be derived from a network-provided timing source, e.g. circuit S.

3) Where the DTE is providing the synchronous network clock, the signal element timing accuracy may have a value differing from ± 0,01 %. In particular for data transmission on primary group band modems, the required accuracy is ± 0,002 % for the data signalling rate of 48 kbit/s and ± 0,005 % for the data signalling rate of 64 kbit/s.

4) Where the DTE provides timing, when directly connected to another DTE, the signal element timing accuracy may be relaxed.

Annex A
(informative)

Classification of timing relationships

The classification of timing relationships into codirectional and contradirectional for the respective circuits is given in table A.1 as an example for circuits in V.24 and X.24 Recommendations. A diagram of those circuits is shown in figure A.1.

Table A.1 — Directional sense of timing relationships

		V.24				X.24	
Timing circuits / **Data and control circuits**		113	114	115	128	X	S
V.24	103	Co-	Contra-				
	104			Co-	Contra-		
X.24	T					Co-	Contra-
	R						Co-

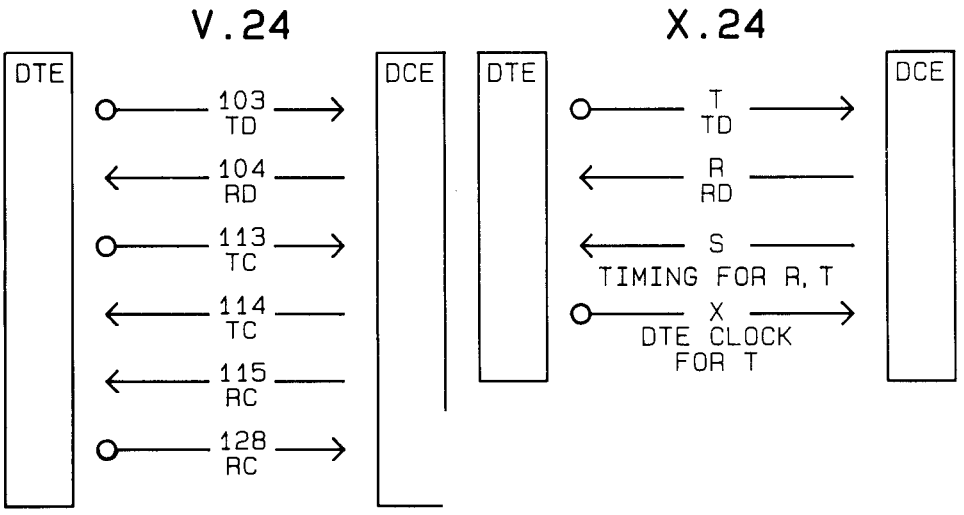


Figure A.1 — Direction of timing and data interchange circuits

UDC 681.327.8 : 621.39 : 621.316.729

Descriptors : data processing, information interchange, transmission.

Price based on 11 pages